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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,779	10/30/2003	Joseph P. Kennedy	1163.00	6911

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EXAMINER	
MOON, SEOKYUN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,779	KENNEDY ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *1 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 1** and **8** are objected to because of the following informalities:

As to **claim 1**, the term "*phase look loop circuit*" is not consistent with the term used in overall portion of application. For further examination purpose, the term will be interpreted as "*phase lock loop circuit*".

As to **claim 8**, the phrase "*wherein said*" is disclosed twice in the claim. For further examination purpose, one of the two phrases will be omitted.

Appropriate correction is required for the claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1**, **2**, and **6** are rejected under 35 U.S.C. 102(e) as being anticipated by Simmonds et al. (U.S. Pat. No. 6,646,645 B2, herein after referred to as "Simmonds").

As to **claim 1**, Simmonds [fig. 3] teaches an image display system for synchronizing the display of images on a plurality of display devices [abstract lines 1-8], comprising:

a first computer system ("*PC 50B*") [fig. 3] generating a first signal representing first image data to be displayed on a first display device ("*PC Graphics Subsystem 60B*");

a second computer system ("*PC 50C*") generating a second signal representing second image data to be displayed on a second display device ("*PC Graphics Subsystems 60C1* and *60C2*"); and

means ("*Sync Card 100*" for "*PC 50B*") for synchronizing said first and second image data [fig. 5], said synchronizing means comprising a phase lock loop circuit ("*PLL 130*") having a digital rate controller to control a lock rate of said phase lock loop circuit (the output of "*PLL 130*" is determined based on the inputted clock value) [col. 8 lines 36-56].

As to **claim 2**, Simmonds [fig. 5] teaches second means ("*Sync Card 100*" for "*PC 50C*") for synchronizing said first and second image data [fig. 5], said synchronizing means comprising a phase lock loop circuit ("*PLL 130*") having a digital rate controller to control a lock rate of said phase lock loop circuit (the output of "*PLL 130*" is determined based on the inputted clock value) of said second synchronization means [col. 8 lines 36-56],

wherein said first synchronizing means ("*Sync Card 100*" for "*PC 50B*") is associated with said first computer system ("*PC 50B*"), said second synchronizing

means ("*Sync Card 100*" for "*PC 50C*") is associated with said second computer system ("*PC 50C*") [fig. 3], and wherein said first and second synchronizing means are synchronized to a master sync signal [col. 7 lines 16-22].

As to **claim 6**, Simmonds teaches said synchronizing means ("*Sync Card 100*" for "*PC 50C*") to be associated with said second computer system ("*PC 50C*") and to synchronize generation of said second signal to said first signal (said second signal is synchronized with a master sync signal which is synchronized with said first signal) [col. 7 lines 16-22].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 3-5** and **7-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmonds in view of Moyal et al. (U.S. Pat. No. 6,704,381 B1, herein after referred to as "Moyal"), and further in view of Miichi (U.S. Pat. No. 5,880,745, herein after referred to as "Miichi").

As to **claim 3**, Simmonds teaches said digital rate controller (internal circuits implemented in "*PLL 130*") comparing / determining whether the inputted signal is master or slave and outputs a signal based on the comparison / determination result [col. 8 lines 36-56].

Simmonds does not disclose expressly the internal structure of said synchronizing means and said phase lock loop circuit.

However, Moyal teaches a phase lock loop comprising:

a phase detector ("*phase frequency detector 52*" which is equivalent to "*phase frequency detector 12*" shown in [fig. 1]) [fig. 3] for comparing said master pulse stream ("*reference clock signal*") to a slave pulse stream ("*feedback signal*") to produce a difference pulse stream [col. 1 lines 33-36];

a low pass filter ("*loop filter 54*" which is equivalent to "*loop filter 14*" shown in [fig. 1]) for filtering said difference pulse stream to produce an analog signal ("*voltage control signal*");

a voltage controlled oscillator ("*80*" which is equivalent to "*voltage controlled oscillator 16*" shown in [fig. 1]) [fig. 3] for producing a clock signal ("*VCO_CLK*") in response to said analog signal ("*voltage control signal*") [col. 1 lines 30-41]; and

said digital rate controller ("*divider 58*") [fig. 3], wherein said digital rate controller divides said clock signal ("*VCO_CLK*") by a divisor value to produce said slave pulse stream ("*feedback signal*"), and wherein said digital rate controller produces said divisor value based on a programmable rate value (the output of the divider which depends on the divisor value is determined based on the setting value of the feedback divider) [col. 5 lines 11-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the internal structure of Simmonds' said synchronizing means and phase lock loop as taught by Moyal to remove the need of a large filter capacitor, the

need of alteration of the charge pump current and to make the charge pump to be non-sensitive to noise [col. 2 lines 43-54].

The modified Simmonds does not disclose a sync separator for receiving said master sync signal and producing a master pulse stream.

However, Miichi [fig. 5] teaches a sync separator ("*input circuit 35*") for receiving said master sync signal ("*the signals inputted from the personal computer 15*") and producing a master pulse stream ("*H/V sync signal*") [col. 8 lines 50-56].

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Miichi's sync separator in the modified Simmonds to filter out the signals such as R, G, B signals that is not directly related to the timing of displaying image and thus allow the modified Simmonds to simplify the synchronization process by only processing the related signals.

As to **claim 4**, Simmonds [fig. 2] teaches said first and second image data to comprise video ("*RGB Analog Video*").

As to **claim 5**, Simmonds [fig. 2] teaches a video generator ("*graphic processor 62*") for generating a video signal in response to said clock signal (the signal that "*sync card 100*" receives).

As to **claim 7**, most of the claim limitations have already been discussed with respect to the rejection of claim 3 except for a sync separator for receiving said first signal.

The modified Simmonds [Simmonds: fig. 3] teaches said sync separators (Miichi: "*input circuit 35*" implemented in Simmonds' "*Sync Card 100*" for "*PC 50C*") for receiving

said first signal (the signal transmitted from "*Sync Card 100*" for "*PC 50B*") [col. 7 lines 23-30].

As to **claim 8**, Simmonds teaches said first and second image data to comprise computer graphics images [abstract lines 8-13].

As to **claim 9**, Simmonds [fig. 2] teaches each of said first and second computer systems further to comprise a graphic processor ("*62*") for generating said computer graphic images [abstract lines 8-13].

As to **claim 10**, Simmonds teaches said graphics processor of said second computer system to generate computer graphics images in response to said clock signal (the signal that "*sync card 100*" receives).

As to **claim 11**, the modified Simmonds as discussed with respect to the rejection of claim 3 teaches an apparatus (Simmonds: "*sync card 100*") for synchronizing to a first digital signal (Simmonds: "*reference clock of the master sync card 100A*"), generation of a second digital signal (Simmonds: "*the reference clock and raster sync signals*" that "*slave sync card 100B*" transmits) [Simmonds:col. 7 lines 16-22], comprising:

a phase detector (Moyal: "*phase frequency detector 52*" which is equivalent to "*phase frequency detector 12*" shown in [fig. 1]) [Moyal: fig. 3] for comparing the first digital signal (Moyal: "*reference clock*") to a comparison pulse stream (Moyal: "*feedback signal*") to produce a difference pulse stream (Moyal: "*pump signals*") [col. 1 lines 33-36];

a low pass filter (Moyal: "*loop filter 54*" which is equivalent to "*loop filter 14*" shown in [fig. 1]) for filtering said difference pulse stream to produce an analog signal (Moyal: "*voltage control signal*");

a voltage controlled oscillator (Moyal: "*80*" which is equivalent to "*voltage controlled oscillator 16*" shown in [fig. 1]) [Moyal: fig. 3] for producing the second digital signal ("*VCO_CLK*") in response to said analog signal (Moyal: "*voltage control signal*") [Moyal: col. 1 lines 30-41]; and

said digital rate controller (Moyal: "*divider 58*") [Moyal: fig. 3], wherein said digital rate controller divides said second digital signal (Moyal: "*VCO_CLK*") by a divisor value to produce said comparison pulse stream (Moyal: "*feedback signal*"), and wherein said digital rate controller produces said divisor value based on a programmable rate value (the output of the divider which depends on the divisor value is determined based on the setting value of the feedback divider) [Moyal: col. 5 lines 11-15] and a comparison of the first digital signal and said comparison pulse stream [Simmonds: col. 8 lines 36-56].

As to **claim 12**, the modified Simmonds [Simmonds: fig. 3] teaches a system for synchronizing video frame rate between a first video system (Simmonds: "PC 50B") displaying video images on a first display device and a second video system (Simmonds: "PC 50C") displaying video images on a second display device [abstract lines 1-8], the system comprising:

a master sync signal generator (Simmonds: "*sync card 100A*"):

a first video input/output module ("*sync card 100B*") associated with said first video system; and

a second video input/output module ("*sync card 100C*") associated with said second video system,

All of the claim limitations regarding the components included in said video input/output modules ("*sync card 100B*" and "*sync card 100C*") have already been discussed with respect to the rejection of claim 3.

As to **claim 13**, all of the claim limitations have already been discussed with respect to the rejection of claim 5.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mukherjee et al. (U.S. Pub. No. 2002/0118201 A1) teaches a system and method for synchronizing image display and buffer swapping in a multiple processor-multiple display environment.

Sakano et al. (U.S. Pub. No. 2002/0159130 A1) teaches a PLL circuit modifying the division ratio of the frequency divider and fixing the ratio at that point to stabilize the frequency of the output clock.

Bontekoe et al. (U.S. Pat. No. 6,078,225) teaches a PLL circuit comprising a loop filter which is a low pass filter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 24, 2006
S.M.

AMR A. AWAD
PRIMARY EXAMINER